SYSTEM BIOS Release Notes
Pineview/Tigerpoint APTIO BIOS

<table>
<tr><td>Date:</td><td>25/02/2010</td></tr>
<tr><td>Name:</td><td>PTMCR042.ROM</td></tr>
<tr><td>System Type:</td><td>Pineview-Tigerpoint Netbook-09 CRB [TigerHill] BIOS</td></tr>
<tr><td>Component List</td><td>Current System Firmware (PNV/TPT): 042

Pineview MRC: 1.12
Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 1 of 2 1.0a
Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 2 of 2 1.0b
Intel® NM10 Express Chipset BIOS Specification 1.5
Integrated VBIOS 1933
PXE OPROM: 4.2.02

Current KSC: 1.11</td></tr>
<tr><td>Description:</td><td>AMI APTIO BIOS for the PNV-TPT based Netbook-09 CRB called TigerHill</td></tr>
<tr><td>How to update:</td><td>1. Using the Dediprog SF100 SPI Flash programmer:
1. Remove the power supply connection to CRB
2. Set Jumpers: J5C3=ON; J4C3=OFF
3. Connect the dediprog to the mother board connector J4C4 (2X4 header) (RED Line of Dediprog should be inline with Pin-1 of the Dediprog Header].
4. Launch the Dediprog Application from your host PC and Make sure that Dediprog is able to detect the onboard SPI part [SST25VF016B]
5. Load the BIOS ROM File and then program the BIOS by clicking the “Batch” Toolbar
6. Once the flashing is done; Set Jumpers: J5C3=OFF; J4C3=ON</td></tr>
<tr><td>Microcode patches included</td><td><table><tr><th>Patch Filename</th><th>CPU</th><th>Patch Version</th></tr><tr><td>M04106CA107</td><td>LCC-SC MB A0 SC Chop</td><td>107</td></tr><tr><td>M04106C9007</td><td>LCC-SC MB A0/A1</td><td>007</td></tr></table></td></tr>
<tr><td>Fixes/Feature updates</td><td>Bug Fixes:

1. MRC updated to ver 1.12 with the IOBuff delay to set before IOBuff Act enable.</td></tr>
<tr><td colspan="2">Release History</td></tr>
<tr><td>PTMCR041.ROM</td><td>BAT Abandoned</td></tr>
</table>

PTMCR040.ROM	**Current System Firmware (PNV/TPT): 040** **Pineview MRC: 1.3** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 1 of 2 1.0a** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 2 of 2 1.0b** **Intel® NM10 Express Chipset BIOS Specification 1.0** **Integrated VBIOS 1933** **PXE OPROM: 4.2.02** **Current KSC: 1.11** **Bug Fixes:** 1. MRC updated to version 1.3 (DDR3 support) **Known Issue**: With 2 DIMMs populated, System cannot able to resume from S3.
PTMCR039.ROM	**Current System Firmware (PNV/TPT): 039** **Pineview MRC: 1.0** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 1 of 2 1.0a** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 2 of 2 1.0b** **Intel® NM10 Express Chipset BIOS Specification 1.0** **Integrated VBIOS 1933** **PXE OPROM: 4.2.02** **Current KSC: 1.10** **Bug Fixes:** 1. MRC rolled back to version 1.0 along with dynamic diffamp disabled. 2. Removed workaround added for Broadcomm HD decoder performance hit issue. 3. Added setup option to display the CPU flavor whether it is Mobile or Desktop. 4. Added S1 feature if it is booted with desktop SKU on Corbett park board. 5. Added setup option to display the memory frequency. 6. Removed Max C-State – C6 option from the setup, since Pineview won't support.

	7. Fixed Self-test failure. Added changes so that, MTRR FIX4K_E0000 region set as WP or UC depends on usage. Note: This BIOS will not support Corbettpark (DDR3) board.
PTMCR038.ROM	BAT Abandoned
PTMCR037.ROM	**Current System Firmware (PNV/TPT): 037** **Pineview MRC: 1.10** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 1 of 2 1.0a** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 2 of 2 1.0b** **Intel® NM10 Express Chipset BIOS Specification 1.0** **Integrated VBIOS 1933** **PXE OPROM: 4.2.02** **Current KSC: 1.10** **Bug Fixes:** 1. MRC Updated to ver 1.10 with DDR3 support 2. Removed workaround to send PowerButton notification during s3 wake. 3. Fixed issue Broadcomm HD Decoder performance hit by adding workaround to disable ASPM L0 for BroadComm. 4. Fixed issue Win7 brightness setting in Power Plan is not working correctly after backlight hotkey pressed. 5. Changed GPIO23 programming to native mode 6. Updated SMBIOS structure to support DDR3. 7. Fixed issue Memory type is not updated properly in setup for DDR3.
PTMCR036.ROM	**Current System Firmware (PNV/TPT): 036** **Pineview MRC: 1.0** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 1 of 2 1.0a** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 2 of 2 1.0b** **Intel® NM10 Express Chipset BIOS Specification 1.0** **Integrated VBIOS 1933** **PXE OPROM: 4.2.02** **Current KSC: 1.10**

	Bug Fixes: 1. VBIOS updated to ver.1933 2. Added Verbtable support for device 10EC/0268 3. Fixed TPT fuse read issue. **Known MRC issue:** 2R X 16 RAWCARD SODIMMS are not working on PNV-D
PTMCR035.ROM	**Current System Firmware (PNV/TPT): 035** **Pineview MRC: 1.0** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 1 of 2 1.0a** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 2 of 2 1.0b** **Intel® NM10 Express Chipset BIOS Specification 1.0** **Integrated VBIOS 1870** **PXE OPROM: 4.2.02** **Current KSC: 1.10** **Bug Fixes:** 1. MRC updated to Ver 1.0 2. Added Microcode patch 107 3. Fixed WHQL issue – Single Compute Display Object test – Laptop 4. Programmed GPIO 29/30/31 as Native as per the Schematics 5. Added multiple verb table support 6. Fixed issue “No sound after ~90cycles in ACPI S3-> S4 test + Quake Game in Win7 OS” 7. Fixed issue WHQL: Tiger Hill Failing UAA Test 8. Fixed issue WHQL: Tiger Hill HD Audio does not have SSVID programmed 9. Cache setting for BIOS Expansion ROM Area i.e. 0xC0000-0xDFFFF and extended BIOS i.e. E0000-E7FFF are changed from WT to WP. **Known MRC issue:** 2R X 16 RAWCARD SODIMMS are not working on PNV-D

PTMCR034.ROM	**Current System Firmware (PNV/TPT): 034** **Pineview MRC: 0.90** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 1 of 2 1.0a** **Intel® Atom™ Processor D500, D400 and N400 Series (Formerly Pineview) BIOS Writer's Guide (BWG) Volume 2 of 2 1.0b** **Intel® NM10 Express Chipset BIOS Specification 1.0** **Integrated VBIOS 1870** **PXE OPROM: 4.2.02** **Current KSC: 1.10** **Bug Fixes:** 1. VBIOS updated to 1870 2. Fixed issue USB thumb disk cannot be detected when Microsoft USB camera connected 3. Updated the DTS threshold table based on TjMax100 4. Added support for BIOS Recovery from USB 5. Fixed some WHQL issue, by adding Powerbutton notification during _WAK method. 6. Clear bit[7:1] of TC/VC0 Map field of VC0 Resource Control register (D27:F0:Reg 114h[7:0]) as per TPT spec. 7. Changed PCI Interrupt Line Register default from 0 to 0xff followed by PCI P2P bridge spec. 8. Reported DTS temperature in TZ01 from 50 degree onwards instead of 60 degree as per the thermal design spec. **Known MRC issue:** 2R X 16 RAWCARD SODIMMS are not working on PNV-D
PTMCR033.ROM	**Current System Firmware (PNV/TPT): 033** **Pineview MRC: 0.90** **Tigerpoint BIOS Specification 0.9** **Pineview Processor BIOS Writer's Guide Voulme-1 0.9a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.9b** **Integrated VBIOS 1851** **PXE OPROM: 4.2.02** **Current KSC: 1.09** **Bug Fixes:** 1. Changed the SSC (Spread Spectrum clock) bios setup option to ON by default **Known MRC issue:** 2R X 16 RAWCARD SODIMMS are not working on PNV-D

PTMCR032.ROM	**Current System Firmware (PNV/TPT): 032** **Pineview MRC: 0.90** **Tigerpoint BIOS Specification 0.9** **Pineview Processor BIOS Writer's Guide Voulme-1 0.9a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.9b** **Integrated VBIOS 1851** **PXE OPROM: 4.2.02** **Current KSC: 1.09** **Bug Fixes :** 1. Removed VREF Margining during S3 resume, just restored the Vref value.
PTMCR031.ROM	**Current System Firmware (PNV/TPT): 031** **Pineview MRC: 0.90** **Tigerpoint BIOS Specification 0.9** **Pineview Processor BIOS Writer's Guide Voulme-1 0.9a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.9b** **Integrated VBIOS 1851** **PXE OPROM: 4.2.02** **Current KSC: 1.09** **Bug Fixes:** 1. Updated to MRC 0.90 a) Performance tuning (T1 dispatch and T2 pull-in) b) RCOMP override algorithm c) Vref margining algorithm d) Remove preproduction values, only support B0 silicon onwards 2. Fixed Linux(Moblin) EHCI handoff issue 3. Added Fast string enabling 4. Updated VBIOS to ver. 1851 5. Updated PXE OpRom to ver. 4.2.02 6. Fixed issue not able to wake from S4 using PCI 7. Changed the implementation of _TMP() in TZ01 to report diode temperature till 60 degree. Above 60 degree, it will give DTS temperature. 8. Implemented Save and Restore Script for HDA VC1 Configuration. 9. Fixed Audio not functioning upon S3 resume. 10. Fixed C4 state missing upon S3 resume. 11. Fixed S4 resume issue in Win7. 12. Fixed issue not booting with PCI IDE card plugged. 13. Fixed issue slow booting if we enable Debug Mode. **This release is for Internal purpose.**

PTMCR030.ROM	**Current System Firmware (PNV/TPT): 030** **Pineview MRC: 0.74** **Tigerpoint BIOS Specification 0.9** **Pineview Processor BIOS Writer's Guide Voulme-1 0.9a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.9b** **Integrated VBIOS 1818** **PXE OPROM: 4.2.02 Beta 1** **Current KSC: 1.07** **Bug Fixes:** 1. Removed all unwanted USB ports disabled setup questions 2. Fixed water ripple issue 3. Fixed issue CPU_STP signal was not toggling 4. Updated to MRC 0.74
PTMCR029.ROM	**Current System Firmware (PNV/TPT): 029** **Pineview MRC: 0.73** **Tigerpoint BIOS Specification 0.9** **Pineview Processor BIOS Writer's Guide Voulme-1 0.9a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.9b** **Integrated VBIOS 1818** **PXE OPROM: 4.2.02 Beta 1** **Current KSC: 1.07** **Bug Fixes:** 1. Fixed Issue Linux OS shows wrong BIOS version. 2. Fixed issue P-States are not happening when HT disabled in PNV Mobile Silicon. 3. Added MCU Patch 105 for Mobile PNV-SC.
PTMCR028.ROM	**Current System Firmware (PNV/TPT): 028** **Pineview MRC: 0.73** **Tigerpoint BIOS Specification 0.9** **Pineview Processor BIOS Writer's Guide Voulme-1 0.9a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.9b** **Integrated VBIOS 1818** **PXE OPROM: 4.2.02 Beta 1** **Current KSC: 1.07**

	Bug Fixes: 1. While entering SMM, Set default cache type to UC and restores it before resume from SMM. 2. Added OSYS=2009 to support Windows 7. 3. Added SMRR setup question in the setup. By default, it is disabled. 4. PROCHOT implementation for SC and DC. 5. VBIOS updated to ver. 1818. This release is for Internal purpose.
PTMCR027.ROM	**Current System Firmware (PNV/TPT): 027** **Pineview MRC: 0.73** **Tigerpoint BIOS Specification 0.9** **Pineview Processor BIOS Writer's Guide Voulme-1 0.9a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.9b** **Integrated VBIOS: 1790** **PXE OPROM: 4.2.02 Beta-1** **Current KSC: 1.07** **Bug Fixes:** 1. Fixed issue clear CMOS using jumper. 2. Fixed issue T2-dispatch enable sequence and limit SODIMM to 667MHz. 3. Updated USB_UHCI token with the correct value. 4. Fixed issue IGD not disabled properly if we set Primary Display to PCI with the PCIe Gfx Card(with/without PCI/PCI bridge) populated in the system. 5. Fixed issue of the COM port not appeared properly in the control panel. 6. Reduced boot time to ~3.2 sec if Fast Boot enabled. 7. Corrected the GM MCH Revision to B0 in the setup. 8. Changed the default critical thermal temperature to 119 Celsius
PTMCR026.ROM	**Current System Firmware (PNV/TPT): 026** **Pineview MRC: 0.71** **Tigerpoint BIOS Specification 0.9** **Pineview Processor BIOS Writer's Guide Voulme-1 0.9a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.9b** **Integrated VBIOS: 1790** **PXE OPROM: 4.2.02 Beta-1** **Current KSC: 1.06** **Feature Updates:** 6. MRC code updated for A0 MB SC RID checking.

	This release is for Internal purpose.
PTMCR025.ROM	**Current System Firmware (PNV/TPT): 025** **Pineview MRC: 0.71** **Tigerpoint BIOS Specification 0.9** **Pineview Processor BIOS Writer's Guide Voulme-1 0.9a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.9b** **Integrated VBIOS: 1790** **PXE OPROM: 4.2.02 Beta-1** **Current KSC: 1.06** **Bug Fixes:** 1. Fixed hang issue at checkpoint 0x96 if we put any card on slot 3 or 2 in Debug Mode in Desktop board. 2. Changed the Processor Family ID to 0x2B (Intel Atom Processor) in the Type4 of SMBIOS table. Previously this ID was 0xB9, which means Pentium Processor.
PTMCR024.ROM	**Current System Firmware (PNV/TPT): 024** **Pineview MRC: 0.71** **Tigerpoint BIOS Specification 0.9** **Pineview Processor BIOS Writer's Guide Voulme-1 0.9a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.9b** **Integrated VBIOS: 1790** **PXE OPROM: 4.2.02 Beta-1** **Current KSC: 1.06** **Feature Updates:** 7. MRC is updated for B0 Silicon stepping 8. Removed CPU FAN Activetrip Point Hi/Lo setup question since it is not PRD. 9. CPU SMRR feature is hidden and disabled by default. **Bug Fixes:** 3. Disabling LAN device from BIOS setup only disables the MAC part of it and PHY is not put to low power mode. This issue is fixed.
PTMCR023.ROM	Internal Release only
PTMCR022.ROM	**Current System Firmware (PNV/TPT): 022** **Pineview MRC: 0.71** **Tigerpoint BIOS Specification 0.9** **Pineview Processor BIOS Writer's Guide Voulme-1 0.9a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.9b** **Integrated VBIOS: 1790** **Current KSC: 1.06** **Feature Updates:**

	1. MRC is updated to v0.71 with following feature/fixes a. New algo for static tRD b. Removed 533MHz related codes c. Renamed “FSB” word to “CoreFreq” as cannot disclose FSB to customers d. Thermal, SCOMP, clock gating, and refresh count registers update e. Code clean up and change version and date. f. For more than 2GB, mobile should hang 2. BIOS support for routing the Port-80 data to PCI or LPC is added 3. Enabled CPU SMRR feature **Bug Fixes:** 1. BIOS support WOL from S5 is added; currently TigerHill CRB supports WOL from S3 only. 4. Disabling LAN device from BIOS setup only disables the MAC part of it and PHY is not put to low power mode. This issue is fixed. 5. Added TGP SATA Link Power Management Errata Workaround. 6. Fixed Replay Timer Timeout error flagged on PCIE port A during S3 by adding logic to continue the code when any of the slot clock bit of all the endpoint functions being set, so that the common clock configuration bit is set for both the rootport and the corresponding endpoint. 7. Revert back MCHBAR 127[7] = 0.
PTMCR021.ROM	**Current System Firmware (PNV/TPT): 021** **Pineview MRC: 0.7** **Tigerpoint BIOS Specification 0.7** **Pineview Processor BIOS Writer's Guide Voulme-1 0.81a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.81a** **Integrated VBIOS: 1772** **Current KSC: 1.06** **Feature Updates:** 1. “Fast boot” option is added to “Boot Menu”; with this option enabled BIOS booting from S4/S5 will be faster. **Bug Fixes:** 1. SATA AHCI boot hang with “Sata Index/data pair decode erratum workaround” is fixed. As a fix to this issue, APTIO AHCI driver is modified to boot without setting the AE bit i.e. ABAR+ offset 04h-bit[31]. 2. SMBIOS Reporting wrong memory size i.e. Memory related Type-17 records are missing in SMBIOS Table. This is fixed 3. BIOS did not set MTRR as WB for remap region (4GB and above). Issue is fixed

	4. Program CI unit when IGD is enabled to qualify the GFX reset bug inherited from BLK-B. 5. WOL from S3/S4 enabled in BIOS but currently TigerHill CRB supports only S3 Wake on LAN. 6. S1 Standby option for Mobile platform is disabled 7. Implemented a workaround to detect the reset triggered by TCO's second timeout 8. SATA Port disable fix is added
PTMCR020.ROM	Internal Release only
PTMCR019.ROM	**Current System Firmware (PNV/TPT): 019** **Pineview MRC: 0.7** **Tigerpoint BIOS Specification 0.7** **Pineview Processor BIOS Writer's Guide Voulme-1 0.81a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.81a** **Integrated VBIOS: 1772** **Current KSC: 1.06** **Feature Updates:** 1. VBIOS is updated to version: 1772 **Bug Fixes:** 1. Fixed SATA AHCI Mode boot hang issue that is seen in BIOS 018. 2. Fixed the issue of MTRR memory region size is not power of 2 due to the size of FV_BB_BLOCKS is 3 or 5 or 6 and also not aligned properly in PEI Phase. 3. Program IGD clock when IGD is secondary display 4. Removed FSB Speed display from the Setup 5. Removed SATA RAID Option from the Setup Changed the BIOS BuildID from B00 to A00 since we are in Alpha Phase
PTMCR018.ROM	**Current System Firmware (PNV/TPT): 018** **Pineview MRC: 0.7** **Tigerpoint BIOS Specification 0.7** **Pineview Processor BIOS Writer's Guide Voulme-1 0.81a** **Pineview Processor BIOS Writer's Guide Voulme-2 0.81a** **Integrated VBIOS: 1758** **Current KSC: 1.06** **Feature Updates:** 6. PXE Boot support via the onboard LAN is enabled. **Bug Fixes:** 1. TPT Power optimization settings enabled. 2. DMI L1 Entry settings enabled. 3. Added all TPT Errata's workaround, except SATA LPM Errata. 4. Mobile Graphics core clock is set to POR frequency of 1667MHZ and whereas the render clock is set to 200MHZ.

	5. Enabled backlight control in VBIOS version 1758 with BMP tool and integrated this in BIOS. This should fix the issue of brightness hot-keys not working issue 6. S3 Resume hang at Post code E1 on Legacy free board is fixed. 7. MRC changes for EDK Compliance
PTMCR017.ROM	**Current System Firmware (PNV/TPT): 017** **Pineview MRC: 0.7** **Tigerpoint BIOS Specification 0.7** **Pineview BIOS specification 0.8** **Integrated VBIOS: 1758** **Current KSC: 1.06** **Feature Updates:** 1. Pineview Mobile SC 007 microcode patch is included 2. MRC 0.7 updated: a. added static tRD and DDR PM features
PTMCR016.ROM	Terminated Release
PTMCR015.ROM	**Component List:** **Current System Firmware (PNV/TPT): 015** **Pineview MRC: 0.61** **Tigerpoint BIOS Specification 0.7** **Pineview BIOS specification 0.8** **Integrated VBIOS: 003** **Current KSC: 1.06** **Feature Updates:** 1. Implemented the setup option to go to either S0/S5 after G3 2. Added support for S1 sleep state. 3. Removed the code which enabled C4 in AC mode. 4. Pineview MRC: a. Performance tuning (clock jitter, LatMax and HWM), b. RDCAMQ token bug fix for B0, c. Power management setting according to DE's recommendation **Bug Fixes:** 1. Fixed issue of power status not updated properly after resume from S4 with Real battery, if Virtual battery switch is set to AC. 2. Fixed issue of LID switch status not getting reported properly to OS if we operate the Lid switch when the system is in Standby mode. 3. Fixed issue "Showing remaining Battery life in OS" 4. Fixed Power Status not updated properly in Windows XP when we connect Real Battery. 5. Send S3/S4/S5 command to EC before entering into Sleep (S4 cycle issue fix). 6. Fixed PNV LVDS DC TDV sighting: see big variation in the VCM

	measured values on tester
PTMCR014.ROM	**Component List:** **Current System Firmware (PNV/TPT): 014** **Pineview MRC: 0.61** **Tigerpoint BIOS Specification 0.5** **Pineview BIOS specification 0.8** **Integrated VBIOS: 0003** **Current KSC: 1.04/1.05** **Feature Update:** 1. Enabled support for Pineview-A1; MRC A0 RID checking is modified to enable A1 support. 2. The static tRD and clock crossing values are updated for all the DDR configurations. 3. Added INT-15 support in BIOS to report the Backlight mode to VBIOS; you need to get the latest VBIOS and flash it for testing this. 4. Enabled Legacy free support in BIOS, capable of booting a board where SIO is not present **Bug Fixes:** 1. EC Lid state isn't getting reported properly on changing the Lid state upon entering S3 –This is fixed, you need to use EC 1.05 2. S4 doesn't wake up on RTC, this issue is fixed and you need to you need to use EC 1.05.
PTMCR013.ROM	**Component List:** **Current System Firmware (PNV/TPT): 013** **Pineview MRC: 0.61** **Tigerpoint BIOS Specification 0.5** **Pineview BIOS specification 0.7** **Integrated VBIOS: 0003** **Current KSC: 1.03** **Feature updates:** 1. Onboard LAN is enabled and tested with WinXP BIOS013 enables Chipset power management settings by default and there is a known bug attached to the released version of Pre-APLHA **Windows Graphics driver** which is related to power management. The moment windows does a C4, with the chipset Power management settings are enabled in BIOS, the graphics driver tries to do some graphics chipset related C4 settings and this is causing a System Hang issue. The issue was root caused to the graphics driver getting into an infinite loop while trying to check for a register-BIT that isn't existed in the PNV-Chipset. In the latest graphics driver they have fixed this issue and this driver is currently under the pre-alpha graphics validation process. You can overcome this issue by either disabling the C-States in BIOS Advanced→CPU menu or by installing the latest PRE-ALPHA Windows Graphics driver which is under validation.
PTMCR012.ROM	**Feature updates:**

	1. Updated new chipset Power Management settings 2. Added new DDR PM settings 3. Added setup options for DMI Power Management 4. Enabled ICH7 LAN Controller HIL 5. Added C-State Popup/C-State Popdown/C4Exit questions in CPU Setup Menu 6. IGDInit library module inclusion: moved Graphics initialization from NBPei.c to IGDInit. **Bug fixes:** 1. Fixed the ACPI Hotkey functionality Issue.(F1 – F4) 2. COM Port is not getting detected under Windows Device Manager; this fixed. 3. MRC Cleanup: same as customer MRC Source 4. With AC97 card plugged in BIOS Boot get stuck at POST Code 78 for 15Sec; this is fixed by modifying the **Counttime** delay routine 5. Jaton PCI Graphics card not working on SVLite board and Mobile CRB.
PTMCR011.ROM	Internal use only
PTMCR010.ROM	**Feature updates:** 7. Enabled IGD Opregion support; DVMT 4.0 support is enabled in BIOS 8. ACPI Hot key support added; enabled support for ctrl+alt+shift F5/F8/F9/F10 Hot keys 9. EC Lid switch toggle notification and Lid switch initial state reporting to graphics driver. 10. USB Wakeup support is added 11. PWM or GMBUS Backlight selection setup option is added 12. Enabled DT/MB DID detection in MRC 13. Updated DMI settings based on DE document and add option to enable power management for NB. 14. Changed DT EV & CRB clock setting Byte3 to Enabled PCIE clock 15. Fixed DMI L1 C3 Control to enable L1 independent of C-states as POR 16. Fixed Traffic class for PCIE root port is incorrect. 17. Fixed MCHBAR offset 0x1C wrong setting (Sighting # 3506099 CPU C-states for graphics) 18. Setup Option for DDR Performance Tuning. 19. Added support for reporting the platform type i.e. MOBILE or DESKTOP to enable the IGD Opregion to report desktop/Mobile implementation specific supported calls. 20. Fix mobile Tx timing value for DDR667 digital 21. Super Sku changes in MRC 22. Updated DMI settings based on DE document and add option to enable power management for NB. **Bug Fixes:** 1. Patcher tool unable to patch the Microcode when BIOS doesn't include any patches in it; this issue was fixed. 2. PCIE Network card not working on Windows XP SP3; fixed this by modifying the IRQ Routing for PCIE Slots 3. Fixed: L1 entry independent of C3/C4; need to set L1C3 control

	bits (DMILINKC register offset 2010 bit [11:10]) to zero 4. Fixed through MCU Patching: Ubuntu 64bit unable to boot on EV DT/MB board 5. AC to DC switch virtual battery switch status is getting updated slowly on windows; fixed this issue. 6. ACPI Hot keys not working: This is fixed through BIOS/EC and latest Graphics driver
PTMCR009.ROM	1. Updated VBIOS to version 003 2. On VISTA with PNV-DC GV3 is happening only on two threads of CORE-0 but not on threads of CORE-1. This issue is fixed by setting the CFGD Bit-23; with this fix _PSD is reporting the right coordination package to OS. 3. Manufacturing mode support is enabled; with this feature BIOS will boot with manufacturing default settings on detecting the manufacturing mode jumper on board. 4. PROCHOT is setting wrong BIT in BIOS; instead of setting BIT 21 of MSR 1A0, it is setting Bit-17 of the same register. This is fixed. 5. CPU Frequency and system bus speed display in BIOS setup is not proper; fixed this with a work around. Issue was MSR CD bit 6..4 is not returning the current FSB Frequency. 6. Removed all Pineview Microcode patches from BIOS 7. Moved TSEG enabling to MRC per MPG request. 8. Moved multiple COMP pulling to the end of 0x27. 9. Updated chipset C2 Settings at 0x23C[15:8]. 10. Fixed memory override timing values. 11. Added Azalia audio codec to fix slow boot at PC78. 12. Fixed booting from PCI IDE and Graphics card not getting detected on PBX. 13. HT disable via CPU setup would crash the system boot; this issue has been fixed 14. Single core enable/disable not working: has been fixed
PTMCR007.ROM	1. Enabled C-States support. C1/C2/C4 has been enabled on both AC and battery. 2. Enabled GV3 [Enhanced speed step] Support 3. EC Virtual battery support enabled 4. EC Lid support has been enabled 5. Enabled S3/S4 Support. Please note that we haven't yet tested S3/S4 on a fully loaded system. S3/S4 regression testing is also not yet done. 6. System shutdown issue has been fixed 7. MRC has been updated v 0.6 a. Enabled DDR-667 min delay support b. Updated DDR-667 MCHODT c. Removed PC 0x22 power cycle for A0 stepping only d. Fixed the MRC 2A hang issue on PNV-MB 8. Enabled Chipset Power Management features 9. Enabled support for loading same VBIOS on PNV-MB and PNV-DT. So you can start using the PNV silicon with PNV-DT Device ID on Tigerhill platform 10. Fixed the BIOS SPI NVARAM write issue; this issue was seen when we put a 1MB BIOS image on a 2M SPI Part 11. Enabled BIOS support for TAT Tool

	12. BIOS Setup cleanup – PCIe port 3 & 4 default Enabled 13. Azalia support added, enabled by default 14. Memory size display in BIOS setup is corrected 15. MBI SMI reporting wrong DVMT Memory; this was due to error in Memory sizing in MBI Module. This has been fixed. In release 008 MBI will be replaced with IGDOpregion 16. Fixed the issue of BIOS hanging at PC-63 when we boot the system with 4GB memory. • Known Issues: Currently we are not seeing a significant drop in voltage when the CPU moves from C0→C4; this core voltage is coming ~900mv. This will be debugged further.
PTMCR006.ROM	1. Fixed SMRAM Relocation issue; no need to clear Global SMI Bit by writing '0' to SMIPORT 2. Fixed ACPI OS Boot and installation issue. With fixes 1 and 2 we can install and boot to a ACPI OS 3. PCI and x1 PCIE Ports are working fine; PCIE Port 2 and 3 are disabled by default; you may have to enable them through 'Setup→Chipset--.ICH Devices" Screen 4. Enabled both the SATA Ports and both ports are getting detected in IDE & AHCI Mode 5. Programming the CK505 Clock values; fixed the Graphics flickering issue 6. Enabled PN-DC with HT [Hyper Threading] support. Tested PNV-DC with HT and Without HT/PNV-SC[No HT] configurations 7. Updated VBIOS to 0002 8. Booted to VISTA/ Windows XP, Ubuntu and Moblin 9. Serial Port is working fine 10. USB Ports are working fine; ; few of the USB Port are disabled by default; you may have to enable them through 'Setup→Chipset--.ICH Devices" Screen
PTMCR005.ROM	1. Updated Receive Enable algorithm at PC 0x2A. 2. Fixed Slow Boot issue at PC 0x31. 3. Fixed AP hang issue at PC 0x35 issue. 4. MRC removed safe config for 59C rank population settings. 5. Fixed MRC PC 0x20 hang issue. 6. Changed build id. 7. Enable IGD. 8. Configure IGD as secondary video adapter when PCI card detected. 9. Fix Display Clock Gating issue. 10. Change Render Clock to POR frequency. 11. Change GMBUS to match with Display clock. 12. Fixed SST SPI Write NVRAM issue. 13. Fixed the BIOS Crash in DEBUG Mode. Issue: GPIO-17 & 48 are muxed with BACKLIGT GPIO Pins. So the BIOS BBS pin [RCRB+3410: BIT11..10] values are getting corrupted; WA Added to save this value before programming GPIO. 14. Fixed the PS2 KB issue which is connected to the EC 15. Fixed the Mobile CRB GPIO usage and enabled SATA IDE Boot on Port-0

	16. Fixed Slow boot issue of DEBUG_MODE by completely caching the BOOT Block; this solution is made generic for both DEBUG/NONDEBUG mode
PTMCR003.ROM	Initial PO BIOS Release; untested.